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EXAMINER	
SOUW, BERNARD E	

ART UNIT	PAPER NUMBER
2881	

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

EJC

Office Action Summary	Application No.	Applicant(s)	
	09/583,617	GORUGANTHU ET AL.	
	Examiner	Art Unit	
	Bernard E. Souw	2881	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Appeal Brief 8/18/2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-19 and 22-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-19 and 22-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 May 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Reopening of Prosecution After Appeal Brief or Reply Brief

1. In view of the Appeal Brief filed on 04/21/2005, PROSECUTION IS HEREBY REOPENED. Reason for reopening this prosecution is set forth below.

The previous rejection of claims 28 and 29 contained a misprint, which is now corrected. Note, in the previous office action claims 28 and 29 have been rejected twice: The first rejection is as being obvious over Yoshida as modified by Gauthier et al., Zingher, Nakasuji and Ishihara et al., which was similar to the rejection of claims 26 and 27. This rejection has been corrected with regard to a minor misprint of not including claims 28 and 29 in the statement of the first rejection. However, the alternative or additional rejection, i.e., as being unpatentable over Yoshida in view of Lo et al. (USPAT #6,504,393, hereinafter addressed as Lo'393), remains intact and unaffected.

The following claim rejections are exactly the same as the previous one, except for a minor correction of a misprint regarding claims 28 and 29, which is here corrected by including claims 28 and 29 in the statement of the first rejection under 35 U.S.C. 103(a) as being obvious over Yoshida as modified by Gauthier et al., Zingher, Nakasuji and Ishihara et al. Since there is no new ground of rejection, this office action is again made FINAL.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37

CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

Finality of Last Office Action Withdrawn

2. Upon further considerations the finality of the rejections of the last Office action (06/24/2005) is withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 4-12, 16-19, 21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida (USPAT # 6,137,295) in view of Talbot et al. (USPAT #6,091,249).

► Regarding claims 1, 16 and 17, Yoshida invents a method for analyzing a semiconductor die (2, 3) having silicon-on-insulator (SOI) structure 1s and a back side

opposite circuitry 1f & 1g near a circuit side, as shown in Fig.1 (referring to claims 1, 16 and 20), the method comprising:

- removing substrate 1a shown in Fig.1 from the back side of the semiconductor die and exposing a region 1c of the insulator of the SOI structure, as recited in Col.5/ll.8-13; and
- inducing a detectable response from the exposed region as a function of a portion of the circuitry, as recited in Col.5/ll.19-32, and therefrom, analyzing the die, as recited in Col.5/ll.52-60;
- wherein the step of inducing a detectable response includes the use of an electron beam (EB) 15, as shown by Yoshida in Fig.2 and recited in Col.1/ll.10-13 + 25-33 and in Col.5/ll.19-32 + 53-55; wherein it is to be particularly noted that the term ***EB*** is *specifically defined* as being an "electron beam" by Yoshida in Col.1/line 11, which is to be distinguished from the term "*EB tester*" that includes a (secondary electron) detector 10, as shown in Fig.13 and recited in Col.1/ll.62-67 and Col.2/ll.1-14
- wherein the step of detecting secondary electrons generated by the electron beam and the circuitry for analyzing the semiconductor die is expressly recited by Yoshida in Col.1/ll.25-33 and in Col.5/ll.19-32 + 53-55.

However, Yoshida's device and/or method does not recite to specifically use a scanning electron microscope to analyze the die, although Yoshida is using an electron beam EB 15, as expressly defined in Col.1/line 11, which is to be distinguished from the term "*EB* ***tester***" that includes a (secondary electron) detector 10, as shown in Fig.13 and recited in Col.1/ll.62-67 and Col.2/ll.1-14. The specific use of a scanning electron

microscope (SEM) to generate the electron beam EB (Yoshida's EB 10) and to analyze the die based on the information carried by the secondary electrons (detected by Yoshida's electron detector 10) is rendered obvious by Talbot et al. in Col.3/ll.13-16 & Col.6/ll.59-60, wherein Talbot's method using SEM, as recited, replace(s) Yoshida's method of using an EB-***tester***.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the electron beam part of an SEM to replace Yoshida's EB, and further, to detect the secondary electrons as taught by Talbot et al., as recited above, in place of using Yoshida's EB ***tester***, since an SEM is a versatile apparatus that can be used for a variety of other purposes with high accuracies and a lot of device sophistication such as automated & computerized alignment, optics adjustment and device performance optimization, such as sample imaging and image processing, as compared to the EB ***tester*** used by Yoshida, which is usually much simpler and very specific in design and structure, while being also limited in the variety of tasks it is capable to execute.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to design Talbot's apparatus, especially owing to its versatility, as recited above, to include all the functions of Yoshida's EB tester, since such a design is very well within skill in the art.

► Regarding claim 4, the step of analyzing the die by detecting the difference between the secondary electron signals obtained from two selected circuit portions is shown by Yoshida's device 1X in Fig.3, which consists of a plurality of circuit portions

(1s & 1f ~~)~~ of Fig.1, which represents voltage variations across the plurality of circuit portions, resulting in a waveform shown in Fig.3, as recited in Col.5/ll.53-67.

► Regarding claims 5 and 21, the step of obtaining an image of the die that represents variations in voltage across the plurality of circuit portions is recited by Yoshida in Col.5/ll.57-67 and Col.6/ll.1-6, as shown in Fig.3 and Fig.4.

► Regarding claim 6, the step of using a pulsed EB is disclosed by Yoshida in Col.6/ll.1-6.

► Regarding claim 7, the step of using a coupling power supply and inputting electrical signals to the die to generate a response is inherent in Yoshida's, as implicated by the testing set 11 shown in Fig.2, recited in Col.5/ll.53-60, which inherently and conventionally includes a power supply.

As previously indicated, Yoshida's EB-tester, which includes Yoshida's DUT, is here to be replaced by Talbot's testing device that is capable of implementing the same tasks as the original Yoshida's DUT. For simplicity, in this office action these specific tasks and the specific units designed by one of ordinary skill in the art to accomplish those tasks will be hereinafter addressed by their equivalent DUT's tasks and units.

► Regarding claim 8, Yoshida's detectable response is obtained from source/drain region 1e (S/D = diffusion region) shown in Fig.1, as disclosed in Col.5/ll.1-5.

► Regarding claim 9, the step of using the BOX layer 1c in Fig.1 as a dielectric in inducing a detectable response, is disclosed by Yoshida in Col.5/ll.55-63, i.e., the potential waveform and potential contrast image shown in Fig.3.

► Regarding claim 10, the step of removing a portion of the substrate 1a to expose a portion of the BOX 1c is shown by Yoshida in Fig.1 and recited in Col.5/ll.8-32.

► Regarding claim 11, Yoshida's method is a post-manufacturing analysis because the device is analyzed after its manufacture is completed, as recited in Col.6/ll.14-19.

► Regarding claim 12, the electrical stimulus applied to the circuitry in the die is provided by *(Talbot's equivalent of)* the DUT board 12 shown in Fig.2, recited in Col.5/ll.43-48.

► Claims 16 and 17 are apparatus (system) claims reciting limitations that are already rejected along with claim 1. The additional recitation of a detector in claim 17 is shown by Yoshida as numeral 14 in Fig.2, as is inherent in Col.5/ll.56-60.

► Regarding claims 18 and 19, the limitation of using a controller to control the substrate removal in claim 17 is rendered obvious by Yoshida's use of the BOX layer as an etching stop to control the substrate removal process, as recited in Col.5/ll.33-41, specifically in Col.5/line 39.

► Regarding claim 23, the step of using a tester adapter to introduce electrical stimulus to the die is disclosed in *(Talbot's equivalent of)* testing set 11 shown in Fig.2, as recited Col.5/ll.53-60.

4. Claims 13 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Talbot et al., and further in view of Zingher (USPAT #4,443,278), Gauthier et al. (USPAT # 4,172,228), and Nakasuji (USPAT #6,465,783),.

Yoshida as modified by Talbot et al. shows all the limitations of claims 13 and 24, as previously applied to claim 12, i.e., parent to claim 13, except the recitation of inputting signals (to stimulate a response) until a failure is induced in the die.

Whether or not to use *Talbot's modification of* Yoshida's DUT board 12 to stimulate a response until a failure is induced in the die, is a mere matter of deliberate choice, and hence, the step is unpatentable for only involving routine skill in the art, as already brought up in all previous Office Actions. Such a step is also conventional, as recited by Zingher in Col.4/ll.57-60, and further, by Gauthier et al. in Col.1/18-27. Furthermore, such a step is usually inherent in the last stages of semiconductor device manufacturing, as recited by Nakasuji in Col.18/ll.20-22 in reference to Step 17 of Fig.10.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Yoshida's DUT board 12 to stimulate a response until a failure is induced in the die, as taught by Gauthier et al. and Zingher, in order to implement a durability testing in semiconductor device manufacturing process, as taught by Nakasuji, since such testing is important for quality control.

5. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Talbot et al., and further in view of Ishihara et al. (USPAT #6,185,324).

Yoshida as modified by Talbot et al. shows all the limitations of claim 14, as previously applied to the parent claim 12, except the specific recitation of inputting signals in a continuous loop. In most automated processes, inputting signals in a

continuous loop is part of the automation process, which is not patentable, because it merely replaces a conventional method that has been normally implemented manually. *In re Venner*, 120 USPQ 192.

Note that "manually" in this regard means that said step(s) may still be part of an automated or computerized process, but a person is involved for monitoring the process and making quick decision and countermeasure where necessary. By inputting the signals in a continuous loop in a fully automated process, monitoring, decision-making and implementing countermeasure are performed automatically performed by inputting and processing the signals in a continuous loop. Such a practice is well known in the art of semiconductor device manufacturing, as recited by Ishihara et al. in the Abstract and in reference of Fig.1.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the data regarding a semiconductor circuit under test into a fully automated production or testing process by putting the data signals in a continuous loop, in order to provide a semiconductor failure analysis in which the cause of a failure is examined easily, accurately and speedily, as taught by Ishihara et al. in Col.2/ll.30-35.

6. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Talbot et al., and further in view of Lo et al. (USPAT 6,344,750, hereinafter denoted as Lo'750) and Cole, Jr. (USPAT #5,523,694).

Yoshida as modified by Talbot et al. shows all the limitations of claim 5, as previously applied to the parent claim 1, except the recitation of using a non-defective die as a reference. More specifically, Talbot et al. disclose a method for analyzing a semiconductor die using an electron beam from a SEM 20 shown in Fig.1, as recited in Col.5/ll.33-57. Talbot's apparatus and method make use of a defect-free device as reference, as recited in Col.6/ll.65-67.

It would have been obvious to adopt Talbot's use of a non-defective die as a reference in Yoshida's method, since from a single image of a device alone *in the absence of other information*, it is difficult to determine whether or not the device under testing (DUT) contains an error, as implicated by Talbot et al. in Col.6/ll.63-65.

One would have been motivated to compare the equivalent EB image of a DUT with a known, non-defective device, as used by Talbot et al., since a defective die would be much more easily and much more quickly recognized by an operator, especially when the image of the non-defective die is subtracted from the currently measured image of a DUT (die under testing), thus highlighting the defect, as generally known in the art of image processing.

The specific wording "*comparing*" the analysis of the dies is expressly recited by Lo'750 in the Abstract/ll.1-5, whereas Cole, Jr. performs various secondary electron image processing as disclosed in Applicant's specification, including adding, subtracting, enhancing, digitizing, storing and many other steps conventional to image processing, as recited in Col.9/ll.37-49.

It would have been obvious to adopt Lo'750's method of comparing the analysis of the dies while performing Cole's various image processing steps, in order to expedite and simplify the electron beam inspection process of Yoshida as modified by Talbot et al.

7. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Talbot et al., and further in view of Kim et al. (USPAT #2002/0043628A1) and Yamazaki et al. (USPAT #6,038,018).

Yoshida as modified by Talbot et al. shows all the limitations of claim 22, as previously applied to the parent claim 17, except the recitation of a die image showing light and dark areas. The limitation that the image of the die shows light and dark areas, the dark areas being indicative of circuit portions having positive voltage greater that that of the lighter areas, is well known in the art as voltage contrast defects, as recited in a large number of prior arts, e.g., by Talbot et al. as recited in the Abstract/ll.1-19 & Col.6/ll.46-48 and shown in Fig.3a-d, by Kim et al. as recited in the Abstract/ll.1-6 from bottom, and by Yamazaki et al., as recited in Col.1/ll.64-67.

It would have been obvious to adopt Talbot's voltage contrast defect inspection method to show light and dark areas, the dark areas being indicative of circuit portions having positive voltage greater that that of the lighter areas, as taught by Kim et al. and Yamazaki et al., in order to provide a simple and speedy defect analysis so highly desirable in the semiconductor manufacturing industry.

8. Claims 24-***29***, are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Nakasuji, Gauthier et al., Zingher and Ishihara et al.

► Claim 24 recite limitations that form a combination of claim 13 (especially regarding the step of inputting electrical signals to cause a failure in the die, e.g., as part of a durability testing and/or quality control), and claim 14 (especially regarding inputting signals in a continuous loop as part of an automation process of chip inspection, durability test and/or quality control), however, without reciting the limitation of a scanning electron microscope (SEM), the latter being recited by Talbot's.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Yoshida's DUT board 12 to stimulate a response until a failure is induced in the die as taught by Gauthier et al., and Zingher, e.g., as part of a durability testing in a semiconductor device manufacturing process, since such testing is important for quality control, as suggested by Nakasuji.

It would have been further obvious to one of ordinary skill in the art at the time the invention was made to integrate the process by putting the data signals in a continuous loop, in order to integrate Yoshida's as modified by Gauthier et al., Zingher and Nakasuji, in a fully automated process as taught by Ishihara et al. to provide a semiconductor durability testing and/or quality control, in which failure can be examined easily, accurately and speedily, as recited by Isihara et al..

► Claim 25 recites limitations that are the same as claims 1 and 4 combined, however, without the recitation of an SEM, such combination having been previously rejected over Yoshida alone. Claim 25 is therefore obvious over Yoshida as modified

by Gauthier et al., Zingher, Nakasuji and Isihara et al., the four secondary prior arts here necessitated by the dependency on claim 24.

► Claims 26 and 27, both recite exactly the same limitations --word by word-- that are obvious over Yoshida, as recited in Col.6/ll.1-19, however, without the limitation of a scanning electron microscope (SEM) recited by Talbot's. Claims 26 and 27 are therefore obvious over Yoshida as modified by Gauthier et al., Zingher, Nakasuji and Ishihara et al., the four secondary prior arts here necessitated by the dependency on claim 24, such that no new reason and motivation to combine are needed (which are, of course, the same as previously applied on claim 24).

► Claims 28 and 29 are also obvious over Yoshida, as recited in Col.6/ll.7-19, in which logical states are expressly recited in Col.6/ll.11-12, again, without the limitation of a scanning electron microscope (SEM) recited by Talbot's. Similar to claims 26 and 27, claims 28 and 29 are therefore obvious over Yoshida as modified by Gauthier et al., Zingher, Nakasuji and Ishihara et al.

9. Claims 28 and 29 are ***additionally*** rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Lo et al. (USPAT #6,504,393, hereinafter addressed as Lo'393).

► Claim 28 recites mostly the same limitations as claim 24, which has been previously rejected as being obvious over Yoshida, as recited above. However, Yoshida does not expressly recite an electron beam inspecting method specifically used

to inspect the logical states of a plurality of circuit nodes. Lo'393 discloses an electron beam method of testing integrated circuit structures that consist a plurality of nodes, as recited in Col.1/ll.19-36. That the nodes take on logical states is well known in the art, as disclosed, e.g., by Shiragasawa et al. in Col.10/ll.18-20. The electron beam detection of various logical states (of the nodes) is specifically recited by Yoshida in Col.6/ll.7-19.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Yoshida's electron beam inspecting method to inspect the logical states of a plurality of circuit nodes, as taught by Lo'393, since logical states of the nodes can be displayed in black and white contrast, as taught by Yoshida in Col.6/ll.2-6, thus expediting and simplifying defect identifications in a semiconductor device manufacturing process.

► Regarding claim 29, the limitations of detecting a non-positive logical state as a function of detecting an uninhibited emission of secondary electrons, and a positive logical state as a function of an inhibited emission of secondary electrons, are inherently recited by Yoshida in Col.6/ll.1-6 + ll.12-14.

Final Rejection

10. No new ground(s) of rejection is presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP §706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of

this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Response to Applicant's Arguments

11. Applicant's arguments filed with the Appeal Brief filed 08/16/2005 have been fully considered, but they are deemed unpersuasive. The following is Examiner's response to Applicant's arguments.

► Regarding claims 1, 4-19 and 23 (Ground A-E), Applicant's argument based on the alleged destruction of the purpose and operation of the Yoshida ('295) reference if the electron beam is replaced by an SEM is groundless.

At first, Applicant's allegation is not supported by any plausible reason, but only speculated based on wrong premises.

Secondly, it is the electron beam in Yoshida's that is replaced by an electron beam similar to Talbot's, i.e., an electron beam as part of an SEM. The Examiner never meant the entire Talbot's SEM is to be incorporated into Yoshida's electron beam tester. This is clear from the statute of the rejection, i.e., Yoshida in view of Talbot. No person of ordinary skill in the art would ever suggest, or even think, about combining two whole

systems into one single system. Since Talbot et al. expressly recite an SEM to perform circuit testing, as already recited in the previous office actions, specifically in Col.3/ll.13-16 & Col.6/ll.59-60, it would have been obvious to one of ordinary skill in the art to use Talbot's electron beam to replace Yohida's. More importantly, since only Yoshida's electron beam is replaced, all features and/or steps in Yoshida's remain intact, such that Applicant's arguments on page 6 and 7 are totally invalid.

Thirdly, no person of ordinary skill in the art would incorporate Talbot's electron beam into Yoshida's system without appropriate and/or necessary modification of each apparatus, so that they both would function properly in combination. Such modification only involves routine skill in the art, and hence, not patentable.

► Regarding claims 1, 4-12, 16-19, 21 and 23 (Ground A above), Applicant's allegation that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). Some teaching of using an SEM electron beam is already given by Talbot, as recited above.

Applicant's further allegation of a lack of motivation and/or citation of auxiliary teaching is unpersuasive, just by Applicant's own citation of Examiner's reason and motivation: "*a SEM is a versatile apparatus that can be used for a variety of other*

purposes with high accuracies and a lot of device sophistication . . . as compared to the EB tester used by Yoshida (:295 reference), which is usually much simpler and very specific in design and structure, while being limited in the variety of tasks it is capable to execute", which is a general knowledge in the art. In this regard, the rationale to modify or combine the prior arts of Yoshida'295 and Talbot et al., i.e., to use an electron beam from Talbot's SEM to replace Yoshida'295's electron beam, does not have to be expressly stated in the prior arts; in the present case the rationale is reasoned from knowledge generally available to one of ordinary skill in the art. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

This relates to suggestion/motivation in that "having established that this knowledge was in the art, the Examiner could then properly rely on a conclusion of obviousness '*from common knowledge and common sense of the person of ordinary skill in the art without any specific hint or suggestion in a particular reference*'." *In re Bozek*, 416 F.2d 1385, 1390, 163 USPQ 545, 549 (CCPA 1969). As already cited above by Applicant, the reason and motivation to combine Yoshida and Talbot, is derived '*from common knowledge and common sense of the person of ordinary skill in the art without any specific hint or suggestion in a particular reference*'.

► Regarding claims 13 and 24 (Ground B above), Applicant's argument that claim 12 is not a parent claim to claim 24 is based on a misunderstanding of the Examiner's ground for rejection (which does not recite such a dependency). The Examiner only recites claim 12 as being a parent to claim 13, but not to claim 24. However, claim 13

includes all the limitations of its parent claims 12, 11 and 1; these limitations being also recited in the independent claim 24: (a) The limitation of "*a method of analyzing a die having SOI structure*" is also recited in claim 1 (*grand-grand-parent to claim 13*); (b) the limitation of "*removing substrate from the backside ...*" is also recited in claim 1; (c) the limitation of "*directing an electron beam to the exposed region of the insulator and inducing a detectable response therefrom as a function of the portion of the circuitry failing and, therefrom, analyzing the die*," is also recited in claim 1 as "*inducing a detectable response from the exposed region as a function of a portion of the circuitry including using an electron beam and detecting secondary electrons generated in response to the electron beam and the portion of the circuitry and, therefrom, analyzing the die [wherein analyzing the die includes using a scanning electron microscope (SEM)]*", as well as in claim 12 "*analyzing the die includes obtaining a response for electrical stimulus applied to circuitry in the die*"; whereas the limitation of claim 24, "*inputting electrical signals to the die to operate the die in a continuous loop known to cause a failure in a portion of circuitry in the die*" is also recited in claim 13 (dependent on claim 12): "*inputting electrical signals includes inputting signals known to induce a failure in the die*."

Therefore, the rejection of claim 13 (dependent on claims 12, 11 and 1) and claim 24 under the same ground is proper.

► Regarding claims 14, 15 and 22, Applicant's argument that there is no evidence of motivation from the cited reference, it is to be noted that the rationale to modify or combine the prior arts does not have to be expressly stated in the prior arts; in the

present case the rationale is reasoned from knowledge generally available to one of ordinary skill in the art. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

This relates to suggestion/motivation in that "having established that this knowledge was in the art, the Examiner could then properly rely on a conclusion of obviousness '*from common knowledge and common sense of the person of ordinary skill in the art without any specific hint or suggestion in a particular reference*'." *In re Bozek*, 416 F.2d 1385, 1390, 163 USPQ 545, 549 (CCPA 1969).

- Specifically regarding claim 14, Applicant's argument that the examiner's motivation of monitoring the process in an continuous loop to replace a manual process is understood in the art --of course-- to also include cases where manual process is not practical and/or possible because of the process speed exceeds the manual reaction of a personal operator. While this is the most frequent case in semiconductor processing, it does not change the fact that an automated process is directed to replace a manual process; it does not matter whether it is introduced just for operator's convenience or because of necessity, such as in regards of process speed. Therefore, the Examiner rejection in paragraph 4 of the Final Office Action, now paragraph 3 on page 8 recites the wording "*most automated process*", instead of "*all automated process*", as misunderstood and/or misinterpreted by Applicant (highlights and underlines added):

> *In **most automated processes**, inputting signals in a **continuous loop** is part of the automation process, which is not patentable, because it merely replaces a conventional method that has been normally implemented manually. In re Venner, 120 USPQ 192.*

Note that "manually" in this regard means that said step(s) may still be part of an automated or computerized process, but a person is involved for monitoring the process and making quick decision and countermeasure where necessary. By inputting the signals in a continuous loop in a fully automated process, monitoring, decision-making and implementing countermeasure are performed automatically performed by inputting and processing the signals in a continuous loop. Such a practice is well known in the art of semiconductor device manufacturing, as recited by Ishihara et al. in the Abstract and in reference of Fig.1.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the data regarding a semiconductor circuit under test into a fully automated production or testing process by putting the data signals in a continuous loop, in order to provide a semiconductor failure analysis in which the cause of a failure is examined easily, accurately and speedily, as taught by Ishihara et al. in Col.2/ll.30-35.

In the Examiner's explanation cited above, the capability of a person to make quick decision and countermeasure may be --of course-- exceeded by the process speed, especially in semiconductor processing. This is generally known by ordinary skill in the art, which usually does not need extra explanation, as in this prosecution.

Furthermore, an automated monitoring of semiconductor processing is expressly taught by Ishihara et al., as recited above. Ishihara's reason and motivation is thus automatically transferred to the present rejection of claim 14.

For all these reasons, Applicant's specific argument regarding the motivation for using Ishihara's automated monitoring is unpersuasive.

• Specifically regarding claim 14, Applicant's argument that Yoshida is teaching away from using Talbot's non-defective die combined with Cole's comparison method is unpersuasive. Yoshida's method of not-using a non-defective die is not teaching away, because Yoshida's *does **not** prohibit* the use of a non-defective die for comparison. On the other hand, both Talbot and Cole provide sufficient reason and motivation to use a method of comparison with a non-defective die, as recited above.

Therefore, Applicant's specific argument that Yoshida allegedly teaches away from using Talbot's non-defective die combined with Cole's comparison method is unpersuasive.

► Regarding claims 24-27 (Ground F above), Applicant's argument that there is no assertion of correspondence to each of the claimed limitations is groundless, because all the pertinent claim limitations have been addressed in reference to the parent claim 24, complete with assertion of correspondence given in the reasons and motivations for combining the applied references, also with reference to column and line numbers, as expressly given in the previous office action.

In particular, claim 24 has been previously rejected together with claim 13, i.e., in paragraph 3 (previously paragraph 4) as being obvious over Yoshida, Talbot, Zingher, Gauthier et al. and Nakasuji. In that paragraph an assertion of correspondence for claim 24 is recited in details in connection to a similar claim 13. The latter inherently includes the pertinent limitations of its parent claims (i.e., claims 12, 11 and 1), which have been elucidated in details in the Examiner's Response (Ground B) above, and also applicable to claim 24 (for being included in the same rejection). In paragraph 6

(previously paragraph 7) the independent claim 24 is once again rejected as being obvious over the same references Yoshida, Zingher, Gauthier et al. and Nakasuji, but now with Ishihara as an additional reference, while discarding Talbot et al. with an appropriate reason, as recited in paragraph 6 above by the wording "*however, without reciting the limitation of a scanning electron microscope (SEM), the latter being recited by Talbot's*". Consequently, against Applicant's allegations a complete assertion of correspondence has been effectively recited in the Examiner's response regarding Ground F above.

► Regarding claims 28 and 29 (Ground G above), Applicant's allegation that the Examiner ignores the limitation of scanning the electron beam across (of course over the exposed region, since otherwise it would not make sense) is based on a wrong premise: The limitation of scanning the electron beam is recited by the secondary references, i.e., by Gauthier et al. in the Abstract/lines 5-7, by Nakasuji in Col.1/ll.15-16 and by Zingher in Col.7/ll.17-18 and Col.8/ll.27-28.

• Still regarding claims 28 and 29 (Ground G), Applicant's argument that claims 28 and 29 are not included in the statement of rejection on page 12 is unpersuasive, because the rejection is doubled, i.e., once in paragraph 7 in previous office action --*not paragraph 8 as recited by Applicant*-- now paragraph 6 in the present office action, and once again in (previous) paragraph 8 (now paragraph 7). Specifically, claims 28 and 29 are rejected in *BOTH* ways, i.e., *EITHER* included in rejection of previous paragraph 8 (now paragraph 6) over Yoshida in view of Nakasuji, Gauthier et al., Zingher and

Ishihara et al. (*wherein there is obviously a misprint involved*), *OR* the rejection is simply omitted and discarded, and simply reject claims 28 and 29 over Yoshida and Lo et al., as recited in previous paragraph 8 (now paragraph 7). In this Office Action, claims 28 and 29 are rejected twice over different prior art references, as recited above.

A previous *misprint* of not including claims 28 and 29 in the first statement over Yoshida in view of Nakasuji, Gauthier et al., Zingher and Ishihara et al. is corrected, as recited above.

- Still regarding claims 28 and 29 (Ground G), Applicant's argument that "*the word 'reject' is not used for the rejection at page 12 (paragraph number 8)*" as recited in Applicant's Appeal Brief, page 10, 3rd full paragraph, lines 1-4, is essentially groundless and has no substance, whatsoever, because the word "reject" is clearly recited in the Final Rejection, page 12, paragraph 8, which is here copied by the Examiner (bolding and underline added):

> *8. Claims 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Lo et al. (USPAT #6,504,393, hereinafter addressed as Lo'393).*

Therefore, Applicant's argument is invalid, for being simply NOT TRUE.

- Still regarding claims 28 and 29 as presented in the Appeal Brief, page 11, first paragraph, is totally not understandable, because the cited page number and line numbers can not be found. The wording "*logical state*" is clearly recited on page 13, lines 15-19, complete with reference citation of column and line numbers. For clarity, the first six lines of page 13 are here reproduced in its original form:

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.... recited in Col.1/ll.19-36. That the nodes take on logical states is well known in the art, as disclosed, e.g., by Shiragasawa et al. in Col.10/ll.18-20. The electron beam detection of various logical states (of the nodes) is specifically recited by Yoshida in Col.6/ll.7-19.

Consequently, the entire last paragraph Applicant's Appeal Brief is dismissed.

Communications

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bernard E Souw whose telephone number is 571 272 2482. The examiner can normally be reached on Monday thru Friday, 9:00 am to 5:00 pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John R Lee can be reached on 571 272 2477. The central fax phone number for the organization where this application or proceeding is assigned is 571 273 8300 for regular communications as well as for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571 272 5993.

bes
January 11, 2006

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